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| 10/543,097 | 07/22/2005 | Keiichi Kurashina | 2005-1121A | 5697 |

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| EXAMINER | |
|---|---|
| LEADER, WILLIAM T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 1795 | |

| NOTIFICATION DATE | DELIVERY MODE |
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| 03/22/2010 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/543,097 | KURASHINA ET AL. | |
| | Examiner | Art Unit | |
| | WILLIAM T. LEADER | 1795 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 January 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) *1-33 and 45-57* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/22/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of Group II, claims 34-45, in the reply filed on November 3, 2009, is acknowledged. Claims 1-33 and 46-57 are withdrawn from consideration.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 34-39, 41 and 43 are rejected under 35 U.S.C. 102(e) as being anticipated by Economikos et al (US 6,773,570)

4. The Economikos et al patent (hereinafter Economikos) is directed to a process for plating and planarizing a workpiece such as a semiconductor wafer (abstract, column 1, lines 11-23). The wafer 1 is illustrated in figure 1B and has a fine recess 3 for interconnects and is covered with a seed layer 4. .This corresponds to the first step of applicant's claim 34. As shown in figure 2, wafer 1 is mounted on carrier 12 and positioned opposite polishing pad 20. Polishing pad 20 is formed with holes 210 and 220 and is placed on table 10 (column 3, lines 63-65). Plating anodes 201, 202, 203, which are preferably sleeves of electrically conducting material, are placed in the holes (column 3, line 66 to column 7, line 3). Plating solution is pumped from

reservoir 200 through the sleeves into the region between the anodes and seed layer 4 on wafer 1. This corresponds to the second step recited in instant claim 34. The anodes are connected to plating voltage source 250 and plating solution is continuously dispensed on pad 20 while the wafer rotates with respect to the pad (column 4, lines 9-22). This corresponds to the third step of claim 34.

5. In the process of Economikos plating and planarization of the plated layer may be performed sequentially. Electroplating solution is dispensed onto the pad while a first amount of mechanical force is applied on the substrate against the pad to maintain a first spacing between the substrate and the pad. An electroetching solution is then dispensed onto the pad, and the metal on the substrate is electroetched, while a second amount of mechanical force is applied on the substrate against the pad to maintain a second spacing between the substrate and the pad. The electroplating and electroetching may be repeated as a sequence a plurality of times. See column 2, lines 51-67. During the plating process, the wafer carrier is adjusted to apply a downward force on the wafer so that the spacing between the wafer and pad is much less than the boundary layer thickness: L<<BL when plating (column 4, lines 34-39). This inequality includes zero spacing (contact between the wafer and pad). After a step of plating has been conducted, a high anodic reverse voltage is applied in place of the plating voltage, and the downward force on the wafer is reduced so that the spacing between the wafer and pad is much greater than the boundary layer thickness: L>>BL when electroetching (column 5, lines 3-12). This corresponds to the last step of applicant's claim 34 since the change in state of the plating voltage (i.e., the plating voltage is discontinued) and the change of the pressing state of the pad 20 (i.e., the force is reduced) are correlated.

6. With respect to claim 35, the change of pressing state is a change in downward force which results in a change in pressure (pressure = force per unit area).

7. With respect to claim 36 the change of state of the plating voltage is intermittence of plating voltage (i.e. the plating voltage is Economikos is alternated with the etching voltage).

8. With respect to claim 37, when the plating voltage is applied the pressure is relatively increased, and when the plating voltage is not applied the pressure is relatively lowered.

9. With respect to claim 38, the change in the pressing state in Economikos may be between contact and non-contact.

10. With respect to claim 39, the changes in pressure and voltage are synchronized to apply high pressure during application of the plating voltage.

11. With respect to claim independent 41, the wafer 1 is illustrated in figure 1B and has a fine recess 3 for interconnects and is covered with a seed layer 4. .This corresponds to the first step of applicant's claim 41. As shown in figure 2, wafer 1 is mounted on carrier 12 and positioned opposite polishing pad 20. Polishing pad 20 is formed with holes 210 and 220 and is placed on table 10 (column 3, lines 63-65). Plating anodes 201, 202, 203, which are preferably sleeves of electrically conducting material, are placed in the holes (column 3, line 66 to column 7, line 3). This corresponds to the second step of claim 41. Plating solution is pumped from reservoir 200 through the sleeves into the regions between the anodes and seed layer 4 on wafer 1. The anodes are connected to plating voltage source 250 and plating solution is continuously dispensed on pad 20 while the wafer rotates with respect to the pad (column 4, lines 9-22). This corresponds to the third step of claim 34. A first amount of force is applied on the substrate against the pad (column 2, lines 57-61).

12. With respect to claim 43, after the process is finished the wafer is removed (column 5, lines 52-55). When the wafer is removed it is separated from the pad.

13. Claims 44 and 45 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsuda et al (US 6,375,823).

14. The Matsuda et al patent (hereinafter Matsuda) is directed to a method for plating onto a workpiece such as a semiconductor device (abstract, column 1, lines 12-14). The workpiece is shown in figure 2 and has fine recesses and conductive layer 103 which includes a copper seed layer (column 9, lines 50-56). This corresponds to the first step recited in applicant's claim 44. A pad 111 is dipped into a plating bath to impregnate the pad with plating solution (column 10, lines 15-18). The pad is made of a porous material (column 10, lines 3-7) and corresponds to the porous member recited in claim 44. The impregnated pad is brought into tight contact with the conductive layer 103. Anode 112 is provided. See figure 1. This corresponds to the second step of claim 44. Electric current is supplied from power supply 113 to anode 112 to form a copper plating film on the surface of conductive layer 103 (column 10, lines 29-34). This corresponds to the third step of claim 44. Matsuda discloses that the step of forming the film alternates with a step of moving the impregnated pad to a remote location where the plating current is interrupted between the anode and the cathode. This step of moving the pad between plating steps would remove plating solution between the porous pad and the seed layer as recited in claim 44. All steps recited in claim 44 are disclosed by Matsuda.

15. With respect to claim 45, as indicated above, Matsuda discloses that the plating current is interrupted when the porous pad is removed from contact with the seed layer and moved to a remote location.

***Claim Rejections - 35 USC § 103***

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

18. Claims 34-39, 41 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Economikos et al (US 6,773,570) in view of Chadda (US 7,025,860) or Emesh et al (2002/0108861).

19. Economikos is interpreted and applied as above. As previously indicated Economikos utilizes polishing pad 20 (column 3, lines 63-65) in the process of electroplating onto the seed layer of a semiconductor workpiece. While one of ordinary skill in the art would recognize that

polishing pads have a degree of porosity, Economikos does not explicitly state that the polishing pad is porous. If Economikos is interpreted as not disclosing a porous polishing pad, the use of a porous pad would have been obvious in view of Chadda or Emesh.

20. The Chadda patent is directed to a process for the electrochemical deposition and removal of a material on a workpiece surface. See the title and abstract. The workpiece may be a semiconductor wafer (column 1, lines 8-10). Chadda discloses that polishing pads may be made of blown urethane, which contains a large number of voids, or other material such as fiber meshes of felts which are porous (column 3, lines 28-40).

21. The Emesh patent is directed to a method for electrochemical treatment of a workpiece such as a semiconductor wafer (abstract; paragraph [0002]). As shown in figure 4, wafer 60 with a metallized surface 80 is urged against polishing pad 40 by wafer carrier assembly 130 (paragraph [0035]). The polishing pad may be formed from blown polyurethane (paragraph [0044]). A porous polishing pad facilitates transportation of the electrolytic solution to the wafer (paragraph 0045]).

22. The prior art of record is indicative of the level of skill of one of ordinary skill in the art. It would have been obvious at the time the invention was made to have utilized a porous polishing pad as disclosed by Chadda or Emesh in the process of Economikos because transport of the electrolyte solution to the surface of the wafer being processed would have been facilitated.

23. Claims 40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Economikos et al (US 6,773,570) in view of Chadda (US 7,025,860) or Emesh et al

(2002/0108861) as applied to claims 34-39, 41 and 43 above, and further in view of Matsuda et al (US 6,375,823) .

24. Claim 40 additionally recites applying plating voltage after a period of time after the porous contact member is brought into contact with the surface of the seed layer. Claim 42 recites that the porous member and the seed layer are moved relatively before performing plating by flowing current. Economikos is silent as to the sequence of contacting and applying a voltage. Matsuda is interpreted as above. Matsuda discloses that the impregnated pad is brought into tight contact with the seed layer and then a plating current is applied (column 10, lines 26-31). It would have been obvious to have utilized the sequence disclosed by Matsuda in the process of Economikos because plating would not commence until the desired orientation of the parts was obtained.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM T. LEADER whose telephone number is (571) 272-1245. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick J. Ryan can be reached on 571-272-1292. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/William Leader/
March 13, 2010

/PATRICK RYAN/
Supervisory Patent Examiner, Art Unit 1795